Simple Arithmetic and Logic Unit Spec

**ALU 1.0**

Q. Given a simple ALU design. Write a UVM based testbench to verify the design.

-> Design is clocked

-> Reset type is Active High. (Reset when value=1)

-> Send input on current cycle, DUT gives output on next cycle

-> Does not support back-to-back transactions

-> Only four operations supported (ADD, SUB, MULT, DIV)

-> Input A should always be greater or equal to Input B

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| --- | --- | --- | --- |
| **Port Name** | **Type** | **Property** | **Size** |
|  |  |  |  |
| Clock | Input | Wire | 1 bit |
| Reset | Input | Wire | 1 bit |
| A | Input | Wire | 8 bits |
| B | Input | Wire | 8 bits |
| ALU\_Sel | Input | Wire | 4 bits |
| ALU\_Out | Output | Reg | 8 bits |
| CarryOut | Output | Bit | 1 bit |

|  |  |
| --- | --- |
| **ALU\_Sel** | **Operation** |
|  |  |
| 4’b0000 | A + B |
| 4’b0001 | A - B |
| 4’b0010 | A \* B |
| 4’b0011 | A / B |
| 4’b0100 – 4’b1111 | Reserved |